IN THE CLAIMS

What is claimed is:

1. A circuit that selects between at least two power supplies, comprising:

an input receiver coupled to receive an input signal and a drive supply that generates a receiver output signal;

a supply comparator having inputs coupled to the at least two power supplies that generates at least one select signal;

a select circuit coupled to the at least two power supplies and the drive supply; and

a latch coupled to the at least one select signal and to the select circuit.

2. The circuit of claim 1, wherein:

the input receiver further includes a driver circuit that receives the input signal and generates an internal input signal, the driver circuit including at least a first driver transistor having a source coupled to the drive supply and a gate coupled to the input signal.

3. The circuit of claim 2, wherein:

the driver circuit comprises a complementary-metal-oxide-semiconductor (CMOS) type driver.

4. The circuit of claim 2, wherein:

the input receiver further includes a first disable device that isolates the driver circuit from at least one power supply in response to an enable signal.

5. The circuit of claim 2, wherein:

the input receiver further includes a second disable device that couples an output of the driver circuit to the driver supply in response to an enable signal.

6. The circuit of claim 1, wherein:

the select circuit comprises a multiplexer having inputs coupled to the at least two power supplies that is controlled according to an output of the latch.

7. The circuit of claim 1, wherein:

the latch is enabled in response to a power up signal.

8. A method of controlling a power supply path to an input receiver, comprising the steps of:

comparing at least two power supply voltages to one another;

setting a latch to indicate one of the at least two power supplies as a selected supply according to said comparison; and

providing the selected supply to the input receiver according to the setting of the latch.

9. The method of claim 8, wherein:

the step of setting the latch occurs substantially during a power-up of an integrated circuit containing the input receiver circuit.

10. The method of claim 8, wherein:

the step of setting the latch includes setting the latch to indicate the power supply having the lowest magnitude voltage.

11. The method of claim 8, further including:

level shifting an output from the input receiver to generate an output signal that varies between predetermined logic levels regardless of which at least one power supply is selected.

12. An input receiver circuit, comprising:

a comparator circuit that generates a select signal in response to a comparison between at least two power supply voltages;

a select circuit that couples one of the at least one power supply voltages to a drive node according to the select signal; and

a drive circuit that drives an internal input signal between the potential of the drive node and another predetermined potential in

response to an input signal.

13. The input receiver circuit of claim 12, wherein:

the comparator circuit includes a comparator having inputs coupled to the at least two power supplies and an output coupled to a passgate that is enabled in response to a power-up signal having a first value.

14. The input receiver circuit of claim 13, wherein:

the comparator circuit can further include a latch having an input coupled to an output of the passgate, and a latch output that provides the select signal, the latch being enabled in response to the power-up signal having a second value.

15. The input receiver circuit of claim 12, wherein:

the select circuit comprises a first supply transistor having a source-drain path coupled between a first supply voltage and the drive node and a second supply transistor having a source-drain path coupled between a second supply voltage and the drive node.

16. The input receiver circuit of claim 12, wherein:

the drive circuit includes a complementary-metal-oxide-semiconductor (CMOS) type driver having an input coupled to receive the input signal and a driver output node that provides the internal input

signal.

17. The input receiver circuit of claim 16, wherein:

a drive circuit further includes

a first enable device coupled between the CMOS type driver and a power supply that provides a low impedance path when an enable signal has a first value, and

a second enable device coupled between the drive node and the driver output node that provides a low impedance path when the enable signal has a second value.

18. The input receiver circuit of claim 12, further including:

a level shift circuit that receives the internal input signal, the level shift circuit including

a pull-up leg that drives an output node to one of the at least two power supply voltages when the internal input signal has a first value, and

a pull-down leg that drives the output node to a different power supply voltage when the internal input signal has a second value, the different power supply voltage being different from any of the at least two power supply voltages.